WHAT IS CLAIMED IS:

1. A burn-in system comprising:

(a) a temperature controlled zone configured to receive a plurality of cartridges each containing a semiconductor wafer including a plurality of integrated circuits, each of the plurality of cartridges including a rigid probe signal printed circuit board and a probe power printed circuit board substantially parallel to and closely spaced from said rigid probe printed circuit board;

(b) test electronics positioned in a cool zone adjacent to said temperature controlled zone;

(c) power electronics positioned in said cool zone adjacent to said temperature controlled zone;

(d) a first interconnection system connecting said test electronics to said rigid probe signal printed circuit board: and

(e) a second interconnection system connecting said power electronics to said probe power printed circuit board;

said first and second interconnection systems being arranged in a stacked relationship and said probe power printed circuit board having at least a bendable section permitting a portion of said probe power printed circuit board to be spaced a greater distance away from said rigid probe signal printed circuit board proximate to said second interconnection system.

2. The burn-in system of claim 1 in which said test electronics comprise burn-in test electronics and electrical test electronics.

3. The burn-in system of claim 1 additionally comprising:

(f) a transition zone separating said temperature controlled zone and said cool zone.

4. The burn-in system of claim 1 in which test electronics comprise a main signal printed circuit board and an extender circuit board connected to said main signal printed circuit board, first and second printed circuit board connectors respectively mounted on said main signal and extender printed circuit boards, each of said main signal and extender printed circuit boards having a plurality of contact members, said main signal printed circuit board connector having a first plurality of interconnection lines connected to said main signal printed circuit board connector and a second plurality of interconnection lines connected to said plurality of contact members of said main signal printed circuit board, said extender

printed circuit board having a third plurality of interconnection lines connected to said extender printed circuit board connector and a fourth plurality of interconnection lines connected to said plurality of contact members of said extender printed circuit board, said first printed circuit board connector engaging said plurality of contact members of said extender printed circuit board and said second printed circuit board connector engaging said plurality of contact members of said main signal printed circuit board.

5. A test system comprising:

(a) a device under test zone configured to receive a plurality of cartridges each containing a semiconductor wafer including a plurality of integrated circuits, each of the plurality of cartridges including a rigid probe signal printed circuit board and a probe power printed circuit board substantially parallel to and closely spaced from said rigid probe printed circuit board;

(b) test electronics positioned adjacent to said device under test zone;

(c) power electronics positioned adjacent to said device under test zone;

(d) a first interconnection system connecting said test electronics to said rigid probe signal printed circuit board; and

(e) a second interconnection system connecting said power electronics to said probe power printed circuit board;

said first and second interconnection systems being arranged in a stacked relationship and said probe power printed circuit board having at least a bendable section permitting a portion of said probe power printed circuit board to be spaced a greater distance away from said rigid probe signal printed circuit board proximate to said second interconnection system.

6. The test system of claim 1 in which said test electronics comprise electrical test electronics.

7. The test system of claim 6 in which said test electronics additionally comprise burn-in test electronics.

8. A burn-in system comprising:

(a) a temperature controlled zone configured to receive a plurality of cartridges each containing a semiconductor wafer including a plurality of integrated circuits,

(b) test electronics positioned in a cool zone;

(c) power electronics positioned in said cool zone; and

(d) a transition zone separating said temperature controlled zone and said cool zone.

9. The burn-in system of claim 8 in which said test electronics comprise burn-in test electronics and electrical test electronics.

10. The burn-in system of claim 8 in which test electronics comprise a main signal printed circuit board and an extender circuit board connected between said main signal printed circuit board and said transition zone.

11. The burn-in system of claim 10 in which said main signal printed circuit board and said extender circuit board have first and second printed circuit board connectors respectively mounted on said main signal and extender printed circuit boards, each of said main signal and extender printed circuit boards having a plurality of contact members, said main signal printed circuit board connector having a first plurality of interconnection lines connected to said main signal printed circuit board connector and a second plurality of interconnection lines connected to said plurality of contact members of said main signal printed circuit board, said extender printed circuit board having a third plurality of interconnection lines connected to said extender printed circuit board connector and a fourth plurality of interconnection lines connected to said plurality of contact members of said extender printed circuit board, said first printed circuit board connector engaging said plurality of contact members of said extender printed circuit board and said second printed circuit board connector engaging said plurality of contact members of said main signal printed circuit board.

12. A test system comprising:

(a) a device under test zone configured to receive a plurality of cartridges each containing a semiconductor wafer including a plurality of integrated circuits;

(b) test electronics on a first circuit board positioned adjacent to said device under test zone;

(c) power electronics on a second circuit board positioned adjacent to said device under test zone;

each of said plurality of cartridges being connected to said test electronics by a first connection between one of said plurality of cartridges and said first circuit board and to said power electronics by a second connection between said one of said plurality of cartridges and

said second circuit board separate from the first connection.

13. The test system of claim 12 in which said test electronics comprise electrical test electronics.

14. The test system of claim 13 in which said test electronics additionally comprise burn-in test electronics.

15. A test system comprising:

(a) a first plurality of test channels each adapted to receive a second plurality of integrated circuits under test;

(b) a second plurality of power modules, each connected to one of the integrated circuits under test in each test channel;

(c) a controller connected and configured for successive selection of one of said first plurality of test channels.

16. The test system of claim 12 in which said test channels comprise electrical test channels.

17. The test system of claim 13 in which said test channels additionally comprise burn-in test channels.

18. The test system of claim 15 in which said power modules each comprise a power input coupled to a device under test output by a switch, a microcontrol element coupled to a control terminal for said switch, a channel select multiplexer coupled to receive a control input from said microcontrol element, and a voltage and current multiplexer coupled to receive a control input from said microcontrol element, said channel select multiplexer being coupled to provide voltage and current measurements from a selected one of said integrated circuits under test to said voltage and current multiplexer, said voltage and current multiplexer being configured to supply the voltage and current measurements to said microcontrol element.

19. The test system of claim 18 in which said voltage and current multiplexer is coupled to receive the control input from said microcontrol element through an analog to digital converter.

20. The test system of claim 18 in which said switch is a metal oxide silicon field effect transistor switch.

21. The test system of claim 18 in which said switch comprises an adjustable voltage regulator.

22. A method for burn-in testing integrated circuits in wafer form, which comprises:

(a) providing a temperature controlled zone configured to receive a plurality of cartridges each containing a semiconductor wafer including a plurality of integrated circuits,

(b) testing the integrated circuits with test electronics positioned in a cool zone;

(c) providing power to the integrated circuits with power electronics positioned in the cool zone; and

(d) separating the test and power electronics from the temperature controlled zone with a transition zone between the temperature controlled zone and the cool zone.

23. The burn-in testing method of claim 8 in which burn-in testing and electrical testing of the integrated circuits is carried out with the test electronics.

24. A method for testing integrated circuits in wafer form, which comprises:

(a) connecting a first plurality of integrated circuits in a second plurality of test channels;

(b) connecting a first plurality of power modules to one of the integrated circuits under test in each test channel;

(c) successively selecting one of the second plurality of test channels;

(d) testing the first plurality of the integrated circuits in the selected test channel; and

(e) repeating steps (c) and (d) until all of the integrated circuits have been tested.

25. The testing method of claim 12 in which the testing is burn-in testing.

26. The testing method of claim 25 in which the testing additionally comprises electrical testing.